AMENDMENT TO THE CLAIMS

1. (Currently amended) A clock multiplier circuit which outputs a multiple clock having a frequency of a multiplication factor externally given with regard to a reference clock, comprising:

a ring oscillator which oscillates at a [[sufficiently]] higher frequency than that of said multiple clock;

a reference clock counter for counting the sampling output of the reference clock by the output clock of the ring oscillator to obtain [[the]] a count value of the half cycle of the reference clock; and

a multiple clock counter which, in case the value obtained by dividing the count value of the half cycle of said reference clock by said multiplication factor is defined as a multiple count value, inverts the [[output of said]] multiple clock output each time it counts said multiple count value by the output clock of said ring oscillator.

2. (Original) A clock multiplier circuit according to claim 1, wherein said ring oscillator comprises an odd number of inverter stages.

3. (Original) A clock multiplier circuit according to claim 1 or 2, wherein said multiple clock counter starts counting of a multiple count value in synchronization with the inversion per half cycle of said reference clock.

4. (Original) A clock multiplier circuit according any one of claims 1 through 3, further comprising:

an unlock detection circuit;

wherein said multiple clock counter generates a count end pulse each time it counts said multiple count value and that said unlock detection circuit determines detection of an unlock in case said count end pulse is not detected within a cycle of said reference clock and restarts said ring oscillator based on determination of said detection of unlock.